gate coupled its drain. The drain of Ml and the gate of MI are coupled to the supply voltage level Vcc. An n-channel MOSFET M2, has its gate coupled to its drain. The gate and drain of M2 are coupled to the source of MI. An n-channel MOSFET M3, has its gate coupled to its drain. The gate of M3 and the drain of M3 are coupled to the source of M2. An n-channel MOSFET M41 has its drain coupled to the drain of M3. The source of M4 is coupled to the source of M3. The gate of M4 is coupled to be controlled by a control voltage level ENl. An n-channel MOSFET M5, has its gate coupled to the gate of M3. The drain of M5 is coupled to the source of M3. The source of M5 is coupled to a substrate node Vbb. An n-channel MOSFET M6, has its drain coupled to the drain of M5. The source of M6 is coupled to the source of M5 and to the substrate node Vbb. The gate of M6 is coupled to be controlled by a control voltage level EN2. The substrate node Vbb, is coupled to the substrate of a integrated circuit chip on which the substrate voltage regulator circuit is contained.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect addition of new claims 45-47. No claims are amended or cancelled. The specific additions are detailed in the following marked up set of claims.

45. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing a portion of the plurality of diodes.